REMARKS

In the present application, claims 1-51 are pending. Claims 25-38 were withdrawn from consideration. Claims 1, 2, 5-14, 17-24, 39, 40, and 43-51 are rejected. Claims 3, 4, 15, 16, 41 and 42 are objected to. As a result of this response, claims 1-24 and 39-51 are believed to be in condition for allowance.

Claim Rejections – 35 USC § 112

The Examiner rejected claims 2, 14, and 40 for reciting "said other IC". The Examiner asserted that there is insufficient antecedent basis in the claims for the limitation. Applicants respectfully respond that the construction "said other IC" derives proper antecedent basis from the preceding recitation of "another IC". Applicants therefore respectfully traverse the Examiner's grounds for rejection with reference to claims 2, 14, and 40.

Claim Rejections – 35 USC § 102

The Examiner rejected claims 1-2, 5-6, 8-9, 12-14, 17, 20, 23-24, 39-40, 43-44 and 46-47 as being anticipated by Hedberg (5,994,921). With respect to claims 1, 5-6, 12-13, 17, 23-34, 39, and 43-44, the Examiner asserted that Hedberg discloses " a multi-mode Input/Output circuit for transmitting and receiving data between integrated circuits wherein each IC contains at least one of said I/O circuits having at least one of transmitter circuitry (fig. 5/no. 21, fig. 6/no. 21) and receiver circuitry (fig. 6/ no. 22), the IC are constructed with CMOS-based transistors that are selectively interconnected together by switches to operate as two single-ended, voltage mode links, and as a single differential voltage mode link (fig. 5, fig. 6, col.1/ln. 15-29, col. 5/ln. 42-col. 6/ln. 8)." Applicants respectively disagree with the Examiners characterization of the teachings of Hedberg.

Claim 1 recites, in part:

> said I/O circuit being constructed with CMOS-based transistors
> that are **selectively interconnected together by switches to**

> **operate** as two single-ended, current or voltage mode links, **and** as a single differential current or voltage mode link. (emphasis added)

Applicants respectfully assert that Hedberg nowhere teaches or otherwise suggests an "I/O circuit being constructed with CMOS-based transistors that are selectively interconnected together by switches to operate as two single-ended, current or voltage mode links, and as a single differential current or voltage mode link" as recited.

Turning first to the Examiner's citation at col. 1, lines 15-29, Hedberg, in the Background section, asserts:

> Early concepts are DTL (Diode-Transistor Logic), TTL (Transistor-Transistor Logic) and ECL (Emitter Coupled Logic). These employ so called single-ended signalling. More recent concepts often employ a technique called differential signalling, also known as balanced signalling, which uses two signalling wires. Such concepts are DPECL (Differential Pseudo Emitter Coupled Logic), LVDS (Low Voltage Differential Signalling) and GLVDS (Grounded Low Voltage Differential Signalling)

Hedberg therefore states that previous attempts at electrical signaling employed single-ended signaling, while more recent attempts employ differential signaling. There is clearly no suggestion of a single circuit selectively inter-connectable to operate in either a single-ended mode or a differential mode as claimed. It is of further note that, in the Summary section, Hedberg states that "A sender device according to the invention is compatible with receiver devices of several existing signalling concepts, e.g. DPECL, LVDS and GLVDS." Every mention of compatible receiver devices involves a differential signaling regime as mentioned above.

At col. 5, line 42 to col. 6, line 8, there are provided descriptions of Figs. 5 and 6. Both Figs, 5 and 6, and their accompanying descriptions, recite the use of differential signaling schemes as evidenced by the repeated recitation of "different signalling levels". Had the Examiner's citation extended one additional paragraph to recite the concluding

paragraph of the Detailed Description, it would be clearly seen that Hedberg states:

> Various alterations and modifications can be done in the described embodiments of the invention by one having skills in the art, without departing from the scope and the spirit of the invention. For example, voltage values stated in the embodiments are only intended as examples for demonstrating the principles of the invention. Other voltage values may be used without changing the essentials of the invention. **Major principles of the invention apply also to single-ended sender devices. Single-ended signalling is well known in the art.** (emphasis added)

Hedberg clearly states, after describing Figs. 5 and 6, that the described principles could be applied to single-ended sender devices. This assertion serves to affirm that there is not previously described any embodiment incorporating single-ended signaling. In addition, in making such an assertion, Hedberg states only that the principles can be applied to "single-ended sender devices" while making no disclosure of a device exhibiting both single-ended and differential operability as claimed. Hedberg therefore teaches a differential signaling device and extension to single-ended sender devices, but purposefully avoids any reference to a single device selectively operating in both modes as recited in claim 1.

As a result of at least this deficiency in the teachings of Hedberg, Applicants traverse the Examiner's grounds for rejections with regard to claim 1. Claim 1 is therefore in condition for allowance. Independent claim 13 recites "selectively interconnecting together the CMOS-based transistors with switches to operate as two single-ended, current or voltage mode links, and as a single differential current or voltage mode link" and independent claim 39 recites "CMOS-based transistors that are selectively interconnected together by switches to operate as two single-ended, current or voltage mode links, and as a single differential current or voltage mode link". For the reasons discussed above, claims 13 and 39 are likewise in condition for allowance. As all of claims 2, 5-6, 12, 14, 17, 20, 23-24, 40, 43-44, and 46-47 depend on claims 1, 13, and 39, they are likewise in condition for allowance.

Claim Rejections – 35 USC § 103

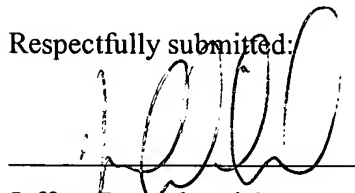
The Examiner rejected claims 7, 10, 11, 18, 19, 21, 22, 45, 48, 49, and 51 as being

unpatentable over Hedberg in view of Pena-Finol et al. (5,832,370). The Examiner further rejected claims 12, 24, and 50 as being unpatentable over Hedberg in view of Bjork et al. (6,009,314).

Applicants respectfully disagree with the Examiner's rejection. Neither Pena-Finol et al. nor Bjork et al. teach, disclose, or otherwise suggest "transistors that are **selectively interconnected together by switches to operate** as two single-ended, current or voltage mode links, **and** as a single differential current or voltage mode link" as claimed in independent claims 1, 13, and 39. For the reasons noted above, Hedberg similarly fails to disclose this claimed element. As a result, the combination of Hedberg with either Pena-Finol et al. or Bjork et al., such a combination neither suggested herein nor deemed appropriate, similarly fails to disclose the element of "transistors that are selectively interconnected together by switches to operate as two single-ended, current or voltage mode links, and as a single differential current or voltage mode link". While Applicants assert no further position on the accuracy of the Examiner's characterization of the teachings of Pena-Finol et al. and Bjork et al., the omission in the cited art of the above noted claimed element is sufficient, by itself, to traverse a rejection to independent claims 1, 13, and 39. As all of claims 7, 10, 11, 18, 19, 21, 22, 45, 48, 49, and 51 are dependent upon claims 1, 13, and 39, they are likewise in condition for allowance.

An early notification of the allowability of claims 1-24 and 39-51 is earnestly solicited.

Respectfully submitted:



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